A ROBUST ULTRA-LOW POWER ASYNCHRONOUS FIFO MEMORY WITH SELF-ADAPTIVE POWER CONTROL

Mu-Tien Chang, Po-Tsang Huang, and Wei Hwang
Department of Electronics Engineering & Institute of Electronics, and Microelectronics and Information Systems Research Center, National Chiao Tung University, HsinChu 300, Taiwan

ABSTRACT
First-in first-out (FIFO) memories are widely used in SoC for data buffering and flow control. In this paper, a robust ultra-low power asynchronous FIFO memory is proposed. With self-adaptive power control and complementary power gating techniques, leakage power of the FIFO memory array is minimized. Moreover, with the proposed dual-V<sub>T</sub> 7T SRAM cell, the FIFO memory has improved stability under ultra-low voltage supply. Simulation results show that the proposed scheme has 16% to 94% power reduction over conventional designs. The proposed scheme is implemented in UMC 90nm CMOS technology under 0.5V supply voltage, with 1.39uW power consumption at 5MHz reading frequency and 200kHz writing frequency.

I. INTRODUCTION
FIFO memory is a key component of many SoC applications, which is commonly used for buffering and flow control. An example is the emerging wireless body area network (WBAN), a breakthrough personal healthcare technology for body condition monitoring and diagnosis. Due to limited energy source and long-term stability requirement, robust ultra-low power designs are indispensable for a WBAN system [1]. As shown in Fig. 1 [2], a major component of the system wireless sensor node (WSN) is a FIFO memory, which dominates the total die area and power. Therefore, reducing power consumption of the FIFO memory is an urgent design consideration for optimal WBAN.

Due to loose timing constraint of the WSN, ultra-low supply voltage is suggested to be an effective method to gain ultra-low power operation. However, in nanometer CMOS technologies, where leakage power contributes a great portion of the total power consumption, the effectiveness of cutting off leakage power by supply voltage scaling is limited. Therefore, further leakage power reduction techniques must be applied to minimize power consumption. Moreover, as supply voltage scales down, CMOS circuit becomes sensitive to noise. Stability issue is especially important for storage elements that operate under ultra-low voltage. Therefore, when designing FIFO memory under ultra-low supply voltage, stability improvement techniques must be applied to ensure functionality. In this paper, three techniques are proposed to gain a robust ultra-low power FIFO memory, including the self-adaptive power control and the complementary power gating for FIFO memory array leakage power minimization, and the dual-V<sub>T</sub> 7T SRAM cell for bitline overhead reduction and data stability improvement.

This paper is organized as follows. The proposed robust ultra-low power FIFO is presented in Section II. Design implementation is shown in Section III. Simulation results and comparisons are shown in Section IV. Finally, conclusions are given in Section V.

II. PROPOSED ROBUST ULTRA-LOW POWER ASYNCHRONOUS FIFO MEMORY
Power and area efficient FIFO memory with simultaneous read/write operation feature can be implemented by separate read/write port SRAM cell array with shift registers as read/write pointers [3]. Fig. 2 shows the block diagram of the proposed FIFO architecture, which is composed by a 7T
SRAM array, read/write shift registers along with read/write control circuitry as logic pointers, read/write circuitry, and adaptive power control circuitry to gain leakage power reduction.

A. Self-adaptive power control

The key idea of leakage power minimization is to reduce voltage swing on un-functioning hardware. To demonstrate this idea, Fig. 3 is an example of FIFO operation. Grey blocks represent words that contain data, while white blocks represent words that are empty. Empty words do not need data retention ability, hence, the cross voltage of the word can be reduced to zero for leakage power minimization. Moreover, due to first-in first-out data behavior, status for each word is completely predictable, i.e., a word changes state only when read or write occurs, where read/write pointer follows circular shifting characteristic, thus allowing self-adaptive power control with acceptable power overhead.

B. Complementary power gating

To support self-adaptive power control, complementary power gating is inserted into each FIFO memory word, as shown in Fig. 4. If the word has data storage, CTRL_CELL is off to turn on the PMOS transistor so that V_VDD has a direct path to VDD for data preservation. On the other hand, if the word is empty, CTRL_CELL is on to turn on the NMOS transistor, so that V_VDD drops to GND, which minimizes the voltage swing across SRAM cells. Complementary power gating is also applied on V_GND, which is the ground of the read buffer of each SRAM cell. When the word is not in read operation, CTRL_READ is off to turn on the PMOS transistor, so that V_GND is boosted to VDD, which minimizes voltage swing between read bitlines and V_GND. If the word is functioning read, CTRL_READ is on to turn on the NMOS transistor so that a read path can be generated. Table 1 summarizes relations between each FIFO memory word status and its corresponding control signals. CTRL_CELL and CTRL_READ are generated by write and read enable signal, no additional control signals are needed.

Complementary power gating ensures no floating node occurs, which promises robust and low leakage operation.
C. Dual-VT 7T SRAM cell

Voltage swing on bitlines is a crucial active power dissipation source in memory architectures. The proposed dual-VT 7T SRAM cell, shown in Fig. 4 features separated single-ended read/write port, which eliminates bitline overhead. However, in ultra-low voltage SRAM design, write ability degrades, where in single-ended write port scheme, the degradation becomes more severe. To compensate the degraded write ability, dual-VT transistors are applied. Due to voltage divider created by M1 and M3, it is more difficult to write data-1, thus, assigning low-VT M1 and high-VT M3 assures the voltage divider effect and improves write ability. Moreover, self-adaptive power control and complementary power gating ensures the empty word to be written into has no data retention ability, which means data on write bitlines can easily write over don’t care data stored in SRAM cells.

Hold stability and read stability are also important for SRAM that operates under ultra-low voltage. Hold stability can be improved by assigning high-VT transistors to the cross coupled inverters M2-M5, since high threshold increases the flipping voltage level, which makes storage nodes more immune to noise. Read stability can be improved by isolating storage nodes from read bitlines during read operation, which is done by inserting read buffer M6-M7.

Comparisons are made between the proposed dual-VT 7T SRAM cell and the conventional dual-port SRAM cell (Fig. 7a) using regular-VT alone, as shown in Fig. 5. Fig. 5 (a) shows that the proposed scheme exhibits better write ability under low supply voltage. Further, Fig. 5 (b) and (c) demonstrate the hold and read stability improvement of the proposed scheme.

III. DESIGN IMPLEMENTATION

A 256-word by 16-bit robust ultra-low power asynchronous FIFO memory is implemented in UMC 90nm CMOS technology with 0.5V supply voltage. The target application is the new generation WBAN, where chip design is required to be highly integrated in a tiny area, and power consumption is limited to μW scale. The proposed design is fully functional within +/-10% voltage variation, 0°C to 100°C temperature variation, and all process corners. The layout view is shown in Fig. 6. Design profile is summarized in Table 2. Power estimation of the FIFO memory is based on the system’s operation characteristic [2], which can be approximately described as:

\[
\text{Power} = 1\% \text{ standby power} + 93\% \text{ write power} + 5\% \text{ simultaneous read/write power} + 1\% \text{ read power}
\] (1)

meaning that 98% of the total time the FIFO is collecting data in a slower rate (200kHz), and 6% of the total time the FIFO outputs data to the WSN signal processor in a faster rate (5MHz).

IV. SIMULATION RESULTS

In this section, power consumption is compared between various kinds of FIFO architecture, including the conventional register based FIFO, existing dual-port SRAM [4-6] based FIFO memories shown in Fig. 7, and the proposed FIFO memory. All of them are implemented in
UMC 90nm CMOS technology with 0.5V supply voltage, but it is worth notice that DP SRAM cell shown in Fig. 7 (a) has weak data preservation ability.

Fig. 8 shows the power consumption comparisons between conventional schemes mentioned above and the proposed scheme. For conventional register based FIFO, although long bitlines don’t exist, a register consumes larger power than an SRAM cell, and the register array size should be two times of a dual-port SRAM array size in order to perform simultaneous read/write, therefore results in much larger power consumption. For conventional dual-port SRAM cell based FIFO memories, bitline overhead and the lack of self-adaptive power control, complementary power gating techniques, result in larger power consumption compared to the proposed scheme.

To sum up, the proposed design has 94%, 79%, 21%, 16%, 16% power reduction compared to conventional register based FIFO, DP SRAM based FIFO, 8T SRAM based FIFO, 10T_C SRAM based FIFO, and 10T_K SRAM based FIFO, respectively.

V. CONCLUSIONS

A robust ultra-low power asynchronous FIFO memory is proposed in this paper. With the self-adaptive power control and complementary power gating technique, leakage power in the FIFO memory array is minimized. Furthermore, to guarantee functionality under low voltage operation, a dual-port dual-V T 7 T  S R A M  c e l l  w i t h  r e d u c e d bitline overhead is proposed to gain stability improvement. Simulation confirms that the proposed design functions successfully under PVT variations with ultra-low supply voltage. The proposed FIFO memory enables robust and ultra-low power operation for future SoC designs.

REFERENCES